REMARKS

In the Claims

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 2 and 5-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *She et al.* in view of *Ahn et al.* (U.S. Patent No. 6,514,828). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *She/Ahn* in view of *Akatsu* (U.S. Patent No. 5,717,635). The Examiner noted that a "product by process" claim is directed to the product *per se,* no matter how actually made. Applicant respectfully traverses this rejection.

Claim 1 has been amended to include a portion of the subject matter of claim 7 – specifically the oxide-oxidized Al-oxide gate dielectric. Claim 7 has been canceled without prejudice.

As is well known in the art, there is a structural difference between an oxidized metal and a chemical vapor deposited metal. The oxidized layer of the present invention is structurally of a higher quality, has a more uniform thickness, and stoichiometric in composition. Chemical vapor deposited layers do not have this type of structure. Therefore, claims of the present invention result in a new product having a different structure than the cited art.

She et al discloses a SONOS-type flash memory using HfO_2 or ZrO_2 as a trapping layer. *She et al.* neither teaches nor suggests Applicant's invention as claimed in the amended claims of an oxide-oxidized Al-oxide gate dielectric. Even if it were assumed that there was no structural difference between an oxidized Al trapping layer and other Al layers formed by other methods, and Applicant maintains that there is such a difference, neither *She, Ahn et al.*, nor *Akatsu* disclose an oxide-Al-oxide gate dielectric.

Ahn et al. discloses an oxidized layer of Hf that is formed over the substrate and oxidized to form an HfO_2 gate oxide layer 62. *Ahn et al.*, at column 6, lines 46 – 51, discloses that a polysilicon layer 64 is then formed over the gate oxide layer 62.

The Examiner states that *Ahn et al.* uses a low-temperature oxidation step to form an oxidized metal gate dielectric similar to She. However, *Ahn et al.* only discloses how to oxidize a

gate oxide layer (layer 62 in Figure 7) and not a metal gate dielectric since the remainder of the gate dielectric of *Ahn et al.* is composed of a polysilicon 64 and a silicide 65. This neither teaches nor suggests Applicant's invention of a gate dielectric of an oxide-oxidized Al-oxide as claimed in the amended claims.

Akatsu only discloses EEPROM arrays that are NOR or NAND type arrays. *Akatsu* neither teaches nor suggests Applicant's invention as claimed in the amended claims.

Even if it were obvious to combine *Ahn et al.* with *She et al.* and/or *Akatsu* and Applicant maintains that it is not, the combination still would not anticipate the present invention as claimed in the amended claims. The combination would yield the oxidized metal tunnel insulator of *Ahn et al.* in combination with the HfO_2 or ZrO_2 trapping layer of *She et al.*

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests that the Examiner withdraw the Final Rejection and allow the present claims. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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